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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,896	04/30/2001	Steven Towle	884.409US1	4065

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/845,896	Applicant(s) TOWLE ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- Th MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 24-35* is/are pending in the application.

4a) Of the above claim(s) *24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 25-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 & 7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-18 and 24-30 in Paper No. 6 is acknowledged.

Claim 24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method claims.

2. Applicant's election with traverse of device claims in Paper No. 6 is acknowledged.

The traversal is on the ground(s) that the restriction requirement based on species is improper.

The restriction based on (paper no. 4) has been withdrawn and the Group I, device claims 1-18 and 25-35 have been examined.

The applicant's arguments with respect to the species restriction requirement are moot since the species restriction requirement has been withdrawn.

Oath/Declaration

3. The oath/declaration filed on 04/30/01 is acceptable.

Drawings

4. The formal drawings filed on 04/30/01 are acceptable.

Information Disclosure Statement

5. The Information Disclosure Statements filed on 04/30/01 and 12/16/02 have been considered.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 4, 6, 7, 18, 25, 27 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Sylvester (US Pat. 6014317).

Regarding claim 1, Sylvester discloses a microelectronic device package/electrical system (10 in Fig. 2) comprising:

- a die (18 in Fig. 2) fixed within a package core/stiffener ring (22 in Fig. 2), the package core being made of a material such as ceramic board/dielectric, metal, etc. (Col. 18, line 35-62)

2; also exposed portion of 56 through solder mask 48 in Fig. 3; Col. 9, line 40-45; Col. 11, line 5-20) built upon the die and the package core, the metalllization layer including a first portion located over/contacting the die and a second portion located over the package core

- a grid array interposer unit/multilayered substrate-MLS (laminated composite including layers 58, 60, 62,50 in Fig. 2) having a plurality of laminations and having a first surface (58 in Fig. 3) laminated to the single/top metallization layer (56 in Fig. 3; Col. 11, line 30), the metallization layer being exposed through a solder mask to provide an electrical connection with solder balls of the device (20 in Fig. 2; Col. 9, line 40)
- the interposer having a first array of electrical contacts/solder balls (42 in Fig. 2) on a second surface, and
- a printed circuit board (PCB 40 in Fig. 2) having a second array of electrical contacts (not numerically referenced in Fig. 2), the respective contacts of the interposer and the PWB being conductively coupled through the solder balls (42 in Fig. 2; Col. 9, line 42)

(Fig. 1-3; Col. 9, line 10- Col. 11, line 60).

Regarding claim 2, as explained above for claim 1, Sylvester discloses the metalllization layer including a first portion located over/contacting the die and a second portion located over the package core

Regarding claim 4, Sylvester further discloses the interposer unit/MLS having a laminate thickness between the first and second surface such as about 2 mils, 3.9 mils, etc. (Col. 3, line 10; Col. 24, line 5), the thickness being no greater than 0.5 mm.

Regarding claim 6, Sylvester discloses the die being fixed within the package core using an encapsulant/resin material (not numerically referenced in Fig. 2- Col. 9, line 66; see filled cavity 30).

Regarding claim 7, as explained above for claim 1, Sylvester discloses a package core being formed from the dielectric material having the metallic cladding on one of the surfaces.

Regarding claim 18, as explained above for claim 1, Sylvester discloses the single metallization layer on the surface of the grid array interposer.

Regarding claim 25, Sylvester discloses substantially the entire claimed structure as applied to the claim 1 above, including an electrical system comprising the die/core and circuit board assembly.

Regarding claim 27, Sylvester discloses substantially the entire claimed structure as applied to the claims 1 and 25 above, including the first array of electrical contacts being a plurality of solder balls.

Regarding claim 32, Sylvester discloses substantially the entire claimed structure as applied to the claims 1 and 4 above, including a connection to the external circuit board/PCB and the grid array interposer unit having a thickness being no greater than 0.5 mm.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 28, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sylvester (US Pat. 6014317) in view of Kelly et al (US Pat. 5798567).

Regarding claim 3, Sylvester discloses substantially the entire claimed structure as applied to the claim 1 above, and further discloses using a capacitor (132 in Fig. 18) connected to the second surface of the grid array interposer unit but fails to specify the capacitor being a decoupling capacitor.

Kelly et al teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the grid array interposer/substrate to improve the electromagnetic interference (EMI) suppression (Col. 4, line 25-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one decoupling capacitor being connected to the second surface of the grid array interposer unit as taught by Kelly et al so that the EMI can be reduced in Sylvester's device.

Regarding claim 28, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above and further discloses a capacitor (132 in Fig. 18) being electrically connected/bonded to the second surface/metallization (126 in Fig. 18) of the grid array interposer unit but fails to specify at least one capacitor being conductively coupled to an exposed portion of the metallization to provide de-coupling for the circuitry within the die.

Kelly et al teach using decoupling capacitors (47 and 67 in Fig. 4 and 5 respectively) being conductively coupled to an exposed portion of the metallization on a top and bottom surfaces of the grid array interposer/substrate (56 and 66 in Fig. 4 and 5 respectively) to provide de-coupling for an integrated circuit to improve the electromagnetic interference (EMI) suppression (Col. 3, line 22-66).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one capacitor being conductively coupled to an exposed portion of the metallization to provide de-coupling for the circuitry within the die as taught by Kelly et al so that the EMI can be reduced in Sylvester's device.

Regarding claim 31, Sylvester discloses substantially the entire claimed structure as applied to claims 1 and 25 above and further discloses a capacitor (132 in Fig. 18) being electrically connected/bonded to the second surface of the grid array interposer unit but fails to specify at least one capacitor being conductively coupled to an exposed portion of the metallization to provide de-coupling for the circuitry within the die.

Kelly et al teach using decoupling capacitors (47 and 67 in Fig. 4 and 5 respectively) being conductively coupled to an exposed portion of the metallization on a top and bottom surfaces of the grid array interposer/substrate (56 and 66 in Fig. 4 and 5 respectively) to provide de-coupling for an integrated circuit to improve the electromagnetic interference (EMI) suppression (Col. 3, line 22-66).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one capacitor being conductively coupled to an exposed portion of the metallization to provide de-coupling for the circuitry within the die as taught by Kelly et al so that the EMI can be reduced in Sylvester's device.

Regarding claim 33, Sylvester discloses substantially the entire claimed structure as applied to claims 1 and 32 above and further discloses using a capacitor (132 in Fig. 18) being electrically connected/bonded to the second surface of the grid array interposer unit but Sylvester fails to specify the capacitor being a decoupling capacitor for providing de-coupling for the circuitry within the die.

Kelly et al teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the grid array interposer/substrate to improve the electromagnetic interference (EMI) suppression (Col. 4, line 25-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one decoupling capacitor being connected to the second surface of the grid array interposer unit to provide de-coupling for the circuitry within the die as taught by Kelly et al so that the EMI can be reduced in Sylvester's device.

10. Claims 8-17 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sylvester (US Pat. 6014317) in view of Harada et al (US Pat. 5523622).

Regarding claim 8, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the details of the routing/pattern of the metaliization/metal cladding providing a ground plane for the transmission structure within the metallization during operation of the device by a conductive coupling of the metal cladding.

Harada et al teach using a metaliization routing/pattern on a die and intermediate substrate (201 and 204 respectively in Fig. 1 and 2) where the metallization is conductively coupled to a plurality of ground planes (206, 207, 209, etc. in Fig. 1 and 2)

through respective ground vias and pads (216 and 218e in Fig. 1, 2 and 5) to provide a ground for the transmission structure, stabilize earth potential and to improve the transmission characteristics (Col. 5, line 1- Col. 6, line 25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal cladding being conductively coupled to a ground providing a ground plane for the transmission structure within the metallization during operation of the device as taught by Harada et al so that the ground potential can be stabilized and the transmission characteristics can be improved in Sylvester's device.

Regarding claim 9, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the details of the routing/pattern of the metaliization/metallic cladding where the metallic cladding is conductively coupled to a power source during device operation to form a power plane.

Harada et al teach using a metaliization routing/pattern on a die and an intermediate substrate (201 and 204 respectively in Fig. 1 and 2) where the metallization is conductively coupled to a power source forming a plurality of power planes (208, 217, etc. in Fig. 1 and 2) through respective power vias and pads to provide the desired routing for the transmission structure (Col. 5, line 1- Col. 6, line 25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal cladding being conductively coupled to a power source during device operation to form a power plane as taught by Harada et al

so that the desired routing for the transmission structure can be achieved and the transmission characteristics can be improved in Sylvester's device.

Regarding claim 10, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the details of the routing/pattern of the metaliization/metallic cladding where the metallization includes at least one ground pad being conductively coupled to the metallic cladding on the package core through one or more vias.

Harada et al teach using a metaliization routing/pattern on a die and an intermediate core substrate (201 and 204 respectively in Fig. 1 and 2) where the metallization includes a plurality of ground pads, vias (218e and 216 respectively in Fig. 1 and 2) and a ground plane (206 in Fig. 1), the metallization being coupled to the respective vias and pads to provide the desired grounding for the transmission structure (Col. 5, line 1- Col. 6, line 25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one ground pad being conductively coupled to the metallic cladding on the package core through one or more vias as taught by Harada et al so that the ground potential can be stabilized and the transmission characteristics can be improved in Sylvester's device.

Regarding claim 11, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the metallization on the die including a

plurality of power bars and ground bars distributed on the surface where each of the power and ground bars being conductively coupled to respective multiple power and ground pads of the die.

Harada et al teach using a metaliization pattern on a die where a plurality of power bars and ground bars are distributed on the surface and interleaved within a central region of the die where each of the power and ground bars (not numerically referenced in Fig. 1- see power and ground bar pattern in the central region) being conductively coupled to respective multiple power and ground pads (218d and 218e in Fig. 1 and 5) of the die (Col. 5, line 57- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of power bars and ground bars distributed on the surface where each of the power and ground bars being conductively coupled to respective multiple power and ground pads of the die as taught by Harada et al so that the ground potential can be stabilized and the transmission characteristics can be improved in Sylvester's device.

Regarding claim 12, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify using a plurality of power bars and ground bars being interleaved within a central region the surface of the die.

Harada et al teach using a metaliization pattern on a die where a plurality of power bars and ground bars are distributed on the surface and interleaved within a central region of the (not numerically referenced in Fig. 1- see power and ground bar

pattern in the central region) to improve the transmission characteristics (Fig. 1 and 5; Col. 5, line 57- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of power bars and ground bars being interleaved within a central region the surface of the die as taught by Harada et al so that the transmission characteristics can be improved in Sylvester's device.

Regarding claim 13, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify a plurality of signal contact pads being distributed within a peripheral region of the surface of the die.

Harada et al teach using a metaliization pattern on the die where a plurality of signal contact pads (218a, and 218b in Fig. 5) is distributed within central and peripheral regions of the surface of the die (Fig. 1 and 5; Col. 5, line 57- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of signal contact pads being distributed within a peripheral region of the surface of the die as taught by Harada et al so that the transmission characteristics can be improved in Sylvester's device.

Regarding claim 14, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the metallization layer including at least power landing pad situated over the die being conductively coupled to multiple power bond pads through corresponding via connections.

Harada et al teach using a metaliization pattern on the die and the substrate where a power landing pad (not numerically referenced - see power landing pad situated above the via connecting the power layer 208 in Fig. 2) is conductively coupled to multiple power bond pads (218d in Fig. 5) through corresponding via connections (216 in Fig. 2; Col. 5, line 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least power landing pad being conductively coupled to multiple power bond pads through corresponding via connections as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Sylvester's device.

Regarding claim 15, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the metallization layer including at least ground landing pad situated over the die being conductively coupled to multiple ground bond pads through corresponding via connections.

Harada et al teach using a metaliization pattern on the die and the substrate where a ground landing pad (not numerically referenced - see ground landing pad situated above the via connecting the ground plane 207 in Fig. 2) is conductively coupled to multiple ground bond pads (218e in Fig. 5) through corresponding via connections (216 in Fig. 2; Col. 5, line 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least ground landing pad situated over the die

being conductively coupled to multiple power bond pads through corresponding via connections as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Sylvester's device.

Regarding claim 16, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the metallization layer including at least power landing pad situated over the package core and being conductively coupled to multiple power bond pads on the die through a trace portion extending over the die and a plurality of via connections.

Harada et al teach using a metaliization pattern on the die and the core substrate where a power landing pad (not numerically referenced - see power landing pad situated above the via connecting the power layer 208 in Fig. 2) is conductively coupled to multiple power bond pads (218d in Fig. 5) through corresponding trace (not numerically referenced in Fig. 5) and via connections (216 in Fig. 2; Col. 5, line 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least power landing pad situated over the package core and being conductively coupled to multiple power bond pads on the die through a trace portion extending over the die and a plurality of via connections as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Sylvester's device.

Regarding claim 17, Sylvester discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the metallization layer including at least one signal landing pad situated over the package core being conductively coupled to a signal bond pad through a path including a transmission line segment.

Harada et al teach using a metaliization pattern on the die and the core substrate where a signal landing pad (not numerically referenced - see signal landing pad on the signal line 203 in Fig. 2 and 3) on the core substrate is conductively coupled to the signal bond pads (218a and 218b in Fig. 5) through a path including a transmission line segment (203 in Fig. 3 and 5; Col. 5, line 1- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one signal landing pad situated over the package core being conductively coupled to a signal bond pad through a path including a transmission line segment as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Sylvester's device.

Regarding claim 35, Sylvester discloses substantially the entire claimed structure as applied to claims 1 and 32 above, but fails to specify including at least ground pad being conductively coupled to the metallic cladding on the package core through one or more via connections.

Harada et al teach using a metallization pattern on the die and the substrate where a ground pad (not numerically referenced - see ground pad situated above the

via connecting the ground plane 207 in Fig. 2) is conductively coupled to multiple ground bond pads (218e in Fig. 5) through corresponding via connections (216 in Fig. 2; Col. 5, line 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least ground pad being conductively coupled to the metallic cladding on the package core through one or more via connections as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Sylvester's device.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sylvester (US Pat. 6014317) in view of Blish, II et al (US Pat. 6049465).

Regarding claim 26, Sylvester discloses substantially the entire claimed structure as applied to claims 1 and 25 above, but fails to specify the first array of contacts including a plurality of pins.

Blish, II et al teach using electrical contacts such as pins (150 in Fig. 1), balls, etc. to provide an external connection between the carrier/interposer and a PWB (Col. 1, line 30-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first array of contacts including a plurality of pins as taught by Blish, II et al so that the integrity and reliability of the external connection can be improved in Sylvester's device.

12. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sylvester (US Pat. 6014317) and Kelly et al (US Pat. 5798567) as applied to claims 1 and 3 above, and further in view of in view of Harada et al (US Pat. 5523622).

Regarding claim 29, Sylvester and Kelly et al teach substantially the entire claimed structure as applied to claims1 and 3 above but fail to specify the metallization layer including at least power landing pad situated over the die being conductively coupled to multiple power bond pads on the die and to a corresponding power contact on the grid array interposer unit.

As explained above for claim 14, Harada et al teach using a metaliization pattern on the die and intermediate substrate (201 and 204 respectively in Fig. 1 and 2) where a power landing pad (not numerically referenced - see power landing pad situated above the via connecting the power layer 208 in Fig. 2) is conductively coupled to multiple power bond pads (218d in Fig. 5) through corresponding power contacts (217 in Fig. 1) on the intermediate substrate (Col. 5, line 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metallization layer including at least power landing pad situated over the die being conductively coupled to multiple power bond pads on the die and to a corresponding power contact on the grid array interposer unit. as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Sylvester's device.

Allowable Subject Matter

13. Claims 5, 30 and 34 are objected to as being dependent upon a rejected base claims 1, 28 and 32 respectively, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach a microelectronic device package comprising: a die fixed within a package core using an encapsulate material; a metalllization layer providing an electrical connection for the die built upon the die and the package core; the metalllization layer including a first portion located over the die and a second portion located over the package core; a grid array interposer unit having a first and second surfaces; the interposer having a first array of electrical contacts on the second surface; a printed circuit board having a second array of electrical contacts; the respective contacts of the interposer and the PWB being conductively coupled through the solder balls; the grid array interposer unit further including an opening that exposes the first portion of the metalllization layer, and at least one capacitor being connected to the first portion of the metalllization layer to provide de-coupling for the circuitry within the die.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
03-05-03

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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